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⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　平1-106456

⑤1Int.Cl.⁴	識別記号	庁内整理番号	⑬公開 平成1年(1989)4月24日
H 01 L 23/50 23/28		G-7735-5F A-6835-5F	

審査請求 未請求 発明の数 1 (全4頁)

⑤4発明の名称　半導体集積回路装置

⑳特　願　昭62-263435

㉒出　願　昭62(1987)10月19日

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明　細　書

1、発明の名称

半導体集積回路装置

2、特許請求の範囲

複数の電極端子を有するリードフレームの一主面の面積が、他の主面より狭く、このリードフレームの断面形状は少なくとも1段以上の段差を持つ段差部を有するものであり、半導体集積回路は他の主面にマウントされ、少なくとも電極端子の一主面を露出した形で一主面とほぼ平坦に封止樹脂が成形されている半導体集積回路装置。

3、発明の詳細な説明

産業上の利用分野

本発明は半導体集積回路をパッケージした半導体集積回路装置に関するものである。

従来の技術

ポータブルな情報ファイルとしてのＩＣカードはカードの一部にメモリ，マイクロプロセッサを有する半導体集積回路装置を埋込んで、リーダーライタを介して情報を書き込み、読み出し、消去する演算機能を持っているが、ＩＳＯ規格によりカード厚みは最大0.84ミリとされており、当然半導体集積回路装置は更に薄くしかも厚み精度が強く要求される。

当初半導体集積回路装置の基板はガラスエポキシを基体とする両面基板が主流であったが、ガラスエポキシ基板ではＩＣカード用半導体集積回路装置に要求する厚み精度を十分に満足させるものではなかった。

そこでガラスエポキシ基板の代りに厚み精度がよく半導体集積回路装置の総厚の厚み精度も向上させられるリードフレームを基板とするＩＣカード用半導体集積回路装置が提案された。このＩＣカード用半導体集積回路装置の構造を第４図に示し説明する。

複数本の電極端子１とダイパッド２を有するリードフレーム８の上記ダイパッド２にＩＣチップ３がマウントされ、上記ＩＣチップ３のパッド（図示せず）と上記電極端子１がワイヤ４で接続されており、少なくとも上記電極端子１の一主面

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5を露出した形で、しかも上記一主面5とほぼ平坦に封止樹脂6がトランスファ成形法により成形された構造となっている。

ところが上記電極端子1の上記一主面5は外部に露出し、上記電極端子1の薄い側面を含む片面しか上記封止樹脂6を接触していない。通常トランスファ成形法で成形する上記封止樹脂6中には成形金型との離形性をよくするために、離形剤が入れられていることから、当然上記電極端子1と上記封止樹脂6との密着性はよいものではない。この問題点を解決する方法として、上記封止樹脂6と接触する他の主面7を粗面化したり、上記電極端子1の一主面5の面積を他の主面7の面積より狭くして(エッジにテーパをつけ台形形状とする)密着性の向上を図っている。

発明が解決しようとする問題点

このような半導体集積回路装置に用いるリードフレーム8の厚味は、半導体集積回路装置に総厚の制限があることから0.15ミリ以下が通常用いられる。ところが封止樹脂6とリードフレーム8の他の主面7との密着性を強化するために、リードフレーム8の断面をテーパ加工し、わずかに封止樹脂6でリードフレーム8を覆う形としているが、リードフレーム8の厚味が0.16ミリと非常に薄いため、封止樹脂6でリードフレーム8の端面を一部覆う形とした場合でもせいぜい厚味分の0.16ミリ程度しか覆うことができず、端面にテーパをつけても封止樹脂6に対するリードフレーム8の密着強度を著るしく向上させることはできなかった。また前にも述べたが封止樹脂6には離形剤が入っているため、リードフレーム8との密着性が悪く、例えば熱衝撃試験を行った時に発生する熱的ひずみによりリードフレーム8が剥れる可能性も生じてくる。更にトランスファ成形後リードフレーム8の補強バーを封止樹脂6の端面に沿ってほぼ平坦に金型にて切断して個片の半導体集積回路装置にするわけであるが、補強バーの切断面は金型で切断する際、わずかなバリが発生することと、完全に封止樹脂6の端面と平坦にすることは不可能で、わずかに切断面が突き出る形となる。この状態でカード化しカードの携帯中あるいは使用中に何らかの異物が切断面にできたバリ、あるいは電極端子自体にひっかかり電極端子をはがしてしまう可能性がある。このように電極端子がはがれたり、変形するとICカードとしての機能が全く失なわれることになる。

本発明は上記問題点を鑑み、外的な力、熱ひずみ等に対しても電極端子がはがれて使用不能にならないようなリードフレームの構造を提供するものである。

問題点を解決するための手段

そして上記問題点を解決する本発明の技術的手段は、リードフレームの一主面の面積を他の主面より狭くし断面形状を凸型として一主面とほぼ平坦に封止樹脂を成形し、リードフレームの端面を所定の距離、厚さでほぼ全辺にわたって封止樹脂で覆うように構成したものである。

作用

この構成により電極端子のほぼ全辺が封止樹脂でおおわれていることから、電極端子を剥す外部からの力が加わらず、また熱衝撃試験等による熱ひずみに対しても電極端子が剥れることがないため信頼性の高い半導体集積回路装置を作ることが可能となる。

実施例

以下本発明の一実施例について図面を用いながら説明する。第2図a,bは本発明に用いたリードフレームの構造を示す。第2図aは上面図、第2図bはA-A'をみた断面図である。ダイパッド11、複数本の電極端子12で構成されており、上記ダイパッド11及び上記電極端子12の外部に露出する一主面13の面積は他の主面14より狭く、少なくとも封止樹脂で覆われる部分のリードフレーム20の断面は凸型の段差部15が設けられている。ちなみにリードフレーム20の肉厚が0.16ミリの場合上記段差部15のWは0.5ミリ、Dは0.1ミリとした。上記段差部15の断面形状は段差が1段のみならず複数段形成されていてもかまわない。以上はダイパッド11が複数本の電極端子12の少なくとも1本と接続されてい

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る構造のリードフレームである。このリードフレーム２００作製方法は一実施例として、まずプレス機でストレートにパンチングした後続いて別の金型を用い同じくプレス機によりリードフレーム２００の端面のみをプレスし所定の量だけ段差部15を作った。他の方法としてエッチングによる方法でも同様の段差部１５を作ることは可能である。以上の説明はＩＣチップを搭載するダイパッド11を有するリードフレーム２０であるが、ダイパッド１１の無い電極端子１２のみのリードフレームでもかまわない。

以上述べた段付きリードフレーム２０を用いた半導体集積回路装置の製造プロセスを第３図ａ～ｃに示す。これは第２図のＡ－Ａ'の断面を表わすものである。ダイパッド１１の他の主面１４にＩＣチップ１６をマウントし、上記ＩＣチップ16のパッド（図示せず）と上記電極端子１２の他の主面１４をワイヤ１７で接続し（第３図ａ）、続いてトランスファ成形法にて上記電極端子１２、及びダイパッド１１の一主面１３を露出させるごとく、上記一主面１３と任意平坦に封止樹脂１８で成形する（第３図ｂ）。この時リードフレーム２０に設けられた段差部１５も上記封止樹脂１８で覆われる形となる。更に金型を用いて上記封止樹脂１８の端面に沿って補強バー１９を切断して個片の半導体集積回路装置とする（第３図ｃ）。以上のべた半導体集積回路装置の電極端子部の拡大図を第１図に示す。この第１図によれば電極端子１２の一主面と封止樹脂１８は任意平坦に成形されており、封止樹脂１８に埋設した電極端子12の一部は、露出している一主面より広がっている構造となっている。このことは、電極端子１２の端面に形成されている段差部１５を完全に封止樹脂１８が覆っていることになり、封止樹脂１８の端面に露出している補強バー１９も同様の凸型であることから外的な力に対しても非常に剥れに強い構造となっている。

以上述べてきた実施例の中でＩＣチップ１６のパッドと電極端子１２の接続にワイヤ１１を用いているが、ワイヤーボンディング法に限定するものではなく、バンプを利用したフリップチップボンディング方式でもかまわない。また同時にリードフレーム２０の他の主面側をエッチング、サンドブラストメッキ法等で粗面化処理が施こされていても良い。更にダイパッド１１が無くＩＣチップ１６が電極端子１２にかかるようなリードフレーム２０を用いる場合はＩＣチップ１６をマウントするダイボンド樹脂は絶縁性であることはいうまでもない。

発明の効果

本発明の半導体集積回路装置はリードフレーム基板の端面に１段以上の段差部を設け、段差部を覆う形で封止樹脂にて成形しているため、外的な力にも電極端子は剥れにくく、熱衝撃試験等の熱ひずみに対しても、電極端子ははがれないことから、信頼性の高いものを得ることが可能となる。

4、図面の簡単な説明

第１図は本発明の半導体集積回路装置の一実施例における電極端子部の拡大斜視図、第２図ａ，ｂは本発明に用いたリードフレームの構造を示す上面図と断面図、第３図ａ～ｃは本発明の半導体集積回路装置の製造フローを示す断面図、第４図は従来のリードフレームを用いた半導体集積回路装置の構造を示す断面図である。

１２……電極端子、１３……一主面、１４……他の主面、１５……段差部、１６……ＩＣチップ、１７……ワイヤ、１８……封止樹脂、１９……補強バー、２０……リードフレーム。

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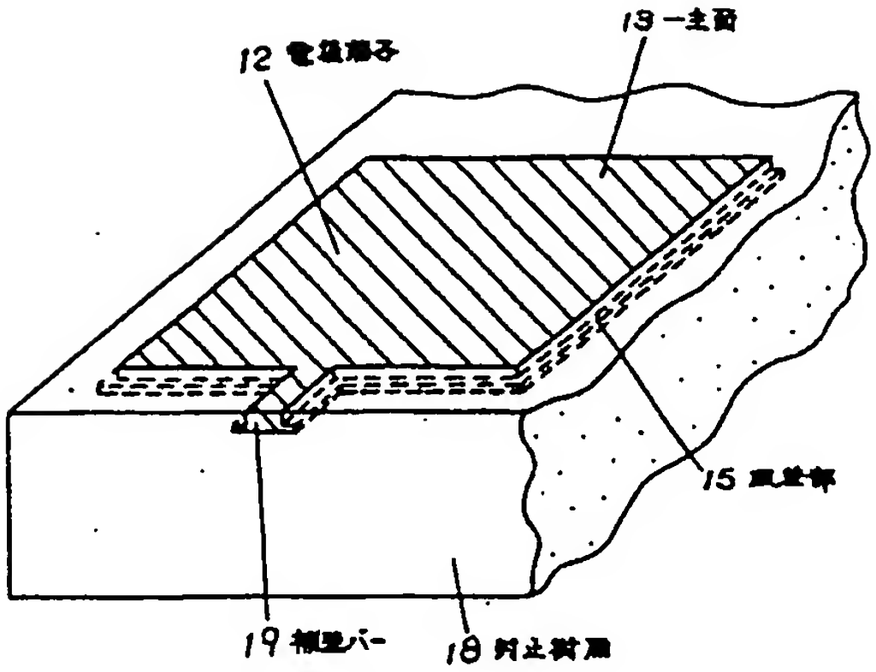
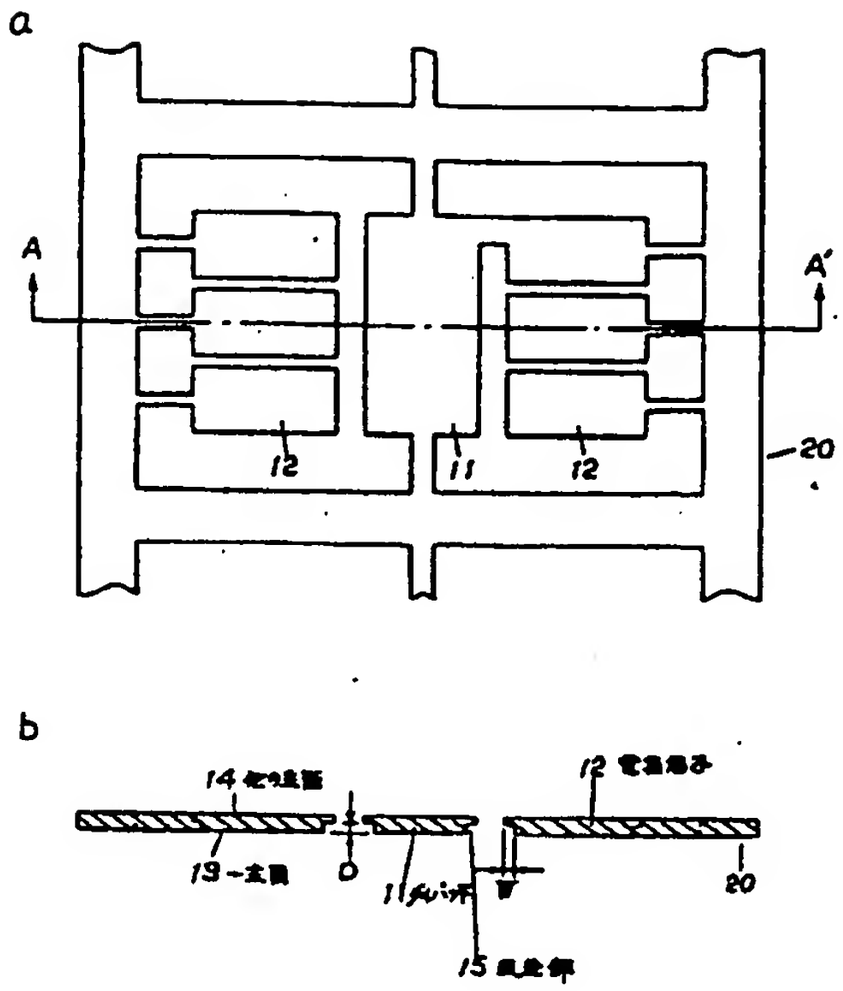
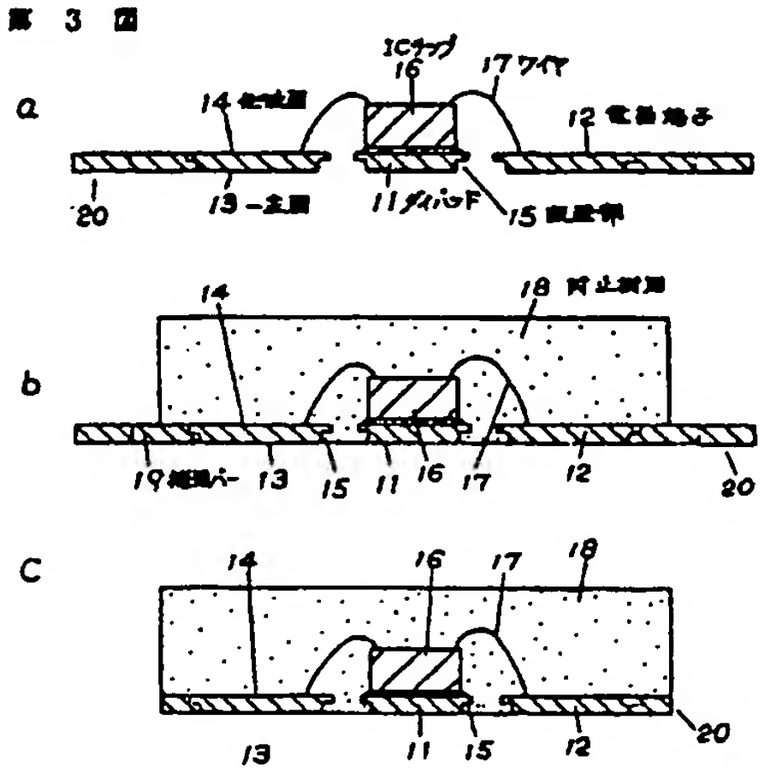
第 1 図



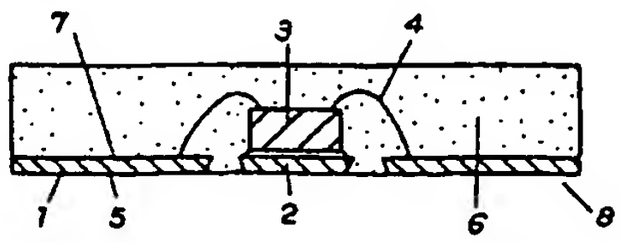
第 2 図



第 3 図



第 4 図



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Japanese Kokai Patent Application No. Hei 1[1989]-106456

Job No.: 2098-96421 Ref.: 022111-000100US
Translated from Japanese by the Ralph McElroy Translation Company
910 West Avenue, Austin, Texas 78701 USA

JAPANESE PATENT OFFICE
PATENT JOURNAL (A)
KOKAI PATENT APPLICATION NO. HEI 1[1989]-106456

Int. Cl.[4]: H 01 L 23/50
23/28

Sequence Nos. for Office Use: G-7735-5F
A-6835-5F

Filing No.: Sho 62[1987]-263435

Filing Date: October 19, 1987

Publication Date: April 24, 1989

No. of Inventions: 1 (Total of 4 pages)

Examination Request: Not filed

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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[There are no amendments to this patent.]

Claim

A semiconductor integrated circuit device characterized by the following facts: the area of one principal surface of a lead frame having plural electrode terminals is smaller than that of the other principal surface; the cross-sectional shape of the lead frame has at least one step; a semiconductor integrated circuit is mounted on the other principal surface; and, with at least said one principal surface having the electrode terminals exposed, molding is performed with a sealing resin so that the resin is nearly flush with said one principal surface.

Detailed explanation of the invention

Industrial application field

The present invention pertains to a semiconductor integrated circuit device containing a packaged semiconductor integrated circuit.

Prior art

An IC card that can be used as a portable information file has a semiconductor integrated circuit device with memory and microprocessor units embedded in a portion of the card. By means of the operation of a reader/writer, information can be written and read or erased. According to the ISO code, the maximum thickness of the card is 0.84 mm. Naturally, the semiconductor integrated circuit device must be even thinner and the thickness must be highly precise.

The conventional substrate for the semiconductor integrated circuit device is usually a double-sided substrate using glass epoxy resin as the base material. However, glass epoxy substrates cannot sufficiently satisfy the demands on thickness precision required for semiconductor integrated circuit devices for IC cards.

Consequently, a semiconductor integrated circuit device for IC cards has been proposed using a lead frame instead of a glass epoxy substrate as a substrate with better thickness precision so as to improve the thickness precision for the overall thickness of the semiconductor integrated circuit device. The structure of this semiconductor integrated circuit device for IC cards can be explained with reference to Figure 4.

For lead frame (8) having plural electrode terminals (1) and die pad (2), IC chip (3) is mounted on said die pad (2), the pad (not shown in the figure) of said IC chip (3) and said electrode terminals (1) are connected by wires (4). With at least one principal surface (5) of said electrode terminals (1) exposed, molding is performed with sealing resin (6) so that the resin is nearly flush with said one principal surface (5) using a transfer molding method.

However, said one principal surface (5) of said electrode terminals (1) is exposed to the outer side, and only one side containing the thin side surface of said electrode terminals (1) contacts said sealing resin (6). Usually, in order to improve the mold releasing property from molding dies in transfer molding methods, a mold releasing agent is added to said sealing resin (6). Naturally, adhesion between said electrode terminals (1) and said sealing resin (6) is not good. Methods for solving this problem include roughening the other principal surface (7) that contacts said sealing resin (6), and making the area of one principal surface (5) of said electrode terminals (1) smaller than the area of the other principal surface (7) (the edge has a tapered, truncated-trapezoid-shape), which improves adhesion.

Problems to be solved by the invention

Due to the limitation on the total thickness of the semiconductor integrated circuit device, the thickness of lead frame (8) used in the semiconductor integrated circuit device is usually 0.15 mm or less. However, in order to improve the adhesion between sealing resin (6) and the other principal surface (7) of lead frame (8), the cross section of lead frame (8) is processed into a tapered shape, and lead frame (8) is covered with a small amount of sealing resin (6). However, the thickness of lead frame (8) is as small as 0.15 mm, so even if the end surface of lead frame (8) is partially covered with sealing resin (6), only about 0.15 mm in thickness is deposited. Even when the end surface is tapered, the adhesive strength of lead frame (8) with respect to sealing resin (6) cannot be increased significantly. Also, as pointed out above, a mold releasing agent is contained in sealing resin (6). Consequently, the adhesion with lead frame (8) is poor. For example, due to thermal strain occurring during the burn-in phase, lead frame (8) may be separated. In addition, after the transfer molding, the reinforcing bar of lead frame (8) is cut by dies nearly flush with the end surface of sealing resin (6) to form individual semiconductor integrated circuit devices. However, when the reinforcing bar is cut by dies to form a cut surface, certain burrs are formed, and it is impossible to form a cut surface that is flush with the end surface of sealing resin (6), and the cut surface protrudes slightly. When a card is formed in this way, when it is carried or in use, certain foreign objects may become caught on the burrs formed on the cut surface or on the electrode terminals themselves. As a result, the electrode terminals may become separated or deformed, leading to total loss of function of the IC card.

The purpose of the present invention is to solve the aforementioned problems of the conventional methods by providing a structure of the lead frame which can avoid separation, and thus failure, of the electrode terminals due to external forces, thermal strain, etc.

Means to solve the problems

In order to solve the aforementioned problem, in the technical means of the present invention, the area of one principal surface of a lead frame is made smaller than the other principal surface; the cross section has a step-like (⊔) shape, and molding is performed with a sealing resin so that the resin is nearly flush with said one principal surface; and, for the end surface of the lead frame, almost the entire edge is covered with the sealing resin over a prescribed distance and thickness.

Operation

In this constitution, since almost the entire edge of the electrode terminals is covered with a sealing resin, no external forces that could separate the electrode terminals can be applied, and no separation takes place in the electrode terminals due to thermal strain during the burn-in phase, etc. Consequently, highly reliable semiconductor integrated circuit devices can be obtained.

Application example

In the following, an application example of the present invention will be explained with reference to the figures. Figures 2a and b illustrate the structure of the lead frame used in the present invention. Figure 2a is a top view, and Figure 2b is a cross-sectional view taken across A-A'. The lead frame is composed of die pad (11) and plural electrode terminals (12). The area of one principal surface (13) exposed on the opposite side of said die pad (11) and said electrode terminals (12) is smaller than the other principal surface (14), and the ⊔ -shaped step (15) is formed as the cross section of lead frame (20) at least in the region to be covered with a sealing resin. When the thickness of lead frame (20) is 0.15 mm, W of said step (15) is 0.5 mm, and D is 0.1 mm. The cross-sectional shape of said step (15) may include plural steps instead of one step. For the aforementioned structure of the lead frame, die pad (11) is connected to at least one of plural electrode terminals (12). As an example for preparing this lead frame (20), first of all, straight punching is performed on a press unit. Then, another set of dies is set on the same press unit and presses just the end surface of lead frame (20) to form step (15) with the prescribed dimensions. In another method, etching is used to form this same step (15). The explanation above is for a lead frame (20) having a die pad (11) that can carry an IC chip. However, it is also possible to use a lead frame having only electrode terminals (12) but without a die pad (11).

Figures 3a-c illustrate the manufacturing process of a semiconductor integrated circuit device using said step-profile lead frame (20). They are taken across A-A' of Figure 2. IC chip (16) is mounted on the other principal surface (14) of die pad (11), and the pad (not shown in the figure) of said IC chip (16) and the other principal surface (14) of said electrode terminals (12)

are connected by wires (17) (Figure 3a). Then, by means of a transfer molding method, where one principal surface (13) of said electrode terminals (12) and die pad (11) is exposed, molding is performed with sealing resin (18) so that the resin is nearly flush with said one principal surface (13) (Figure 3b). At this time, step (15) set on lead frame (20) is also covered with said sealing resin (18). In addition, dies are used to cut reinforcing bar (19) along the end surface of said sealing resin (18) to form individual semiconductor integrated circuit devices (Figure 3c). Figure 1 is an enlarged view of the electrode terminal portion of the aforementioned semiconductor integrated circuit device. According to Figure 1, one principal surface of electrode terminals (12) and sealing resin (18) are formed nearly flush with each other, and a portion of electrode terminals (12) embedded in sealing resin (18) is wider than the exposed one principal surface in this structure. In this way, step (15) formed on the end surface of electrode terminal (12) is completely covered by sealing resin (18), and reinforcing bar (19) exposed on the end surface of sealing resin (18) also has a step-like (⌐¬) shape, so that it is very resistant to separation due to external forces.

As explained above, wires (11) are used for connecting the pad of IC chip (16) to electrode terminals (12). However, the present invention is not limited to the wire bonding method. The flip-chip-bonding method using bumps may also be adopted. Also, at the same time, the other principal surface of lead frame (20) may be processed by etching, sandblasting, or the like to form a rough surface. In addition, when a lead frame (20) without a die pad (11) is used with IC chip (16) and set against electrode terminals (12), the die bonding resin for mounting IC chip (16) is naturally insulating.

Effects of the invention

For the semiconductor integrated circuit device in the present invention, one or several steps are formed on the end surface of the lead frame substrate, and a sealing resin is used for molding to cover the step. Consequently, the electrode terminals cannot be separated even by external forces, and the electrode terminals cannot be separated even by thermal strain during a burn-in phase or the like. That is, high reliability can be realized.

Brief description of the figures

Figure 1 is an enlarged oblique view of the electrode terminal portion in an application example of the semiconductor integrated circuit device of the present invention. Figures 2a and b are a top view and a cross-sectional view illustrating the structure of the lead frame used in the present invention, respectively. Figures 3a-c are cross-sectional views illustrating the manufacturing process of the semiconductor integrated circuit device in the present invention.

Figure 4 is a cross-sectional view illustrating the structure of the semiconductor integrated circuit device using a conventional lead frame.

12 Electrode terminal
13 One principal surface
14 Other principal surface
15 Step
16 IC chip
17 Wire
18 Sealing resin
19 Reinforcing bar
20 Lead frame

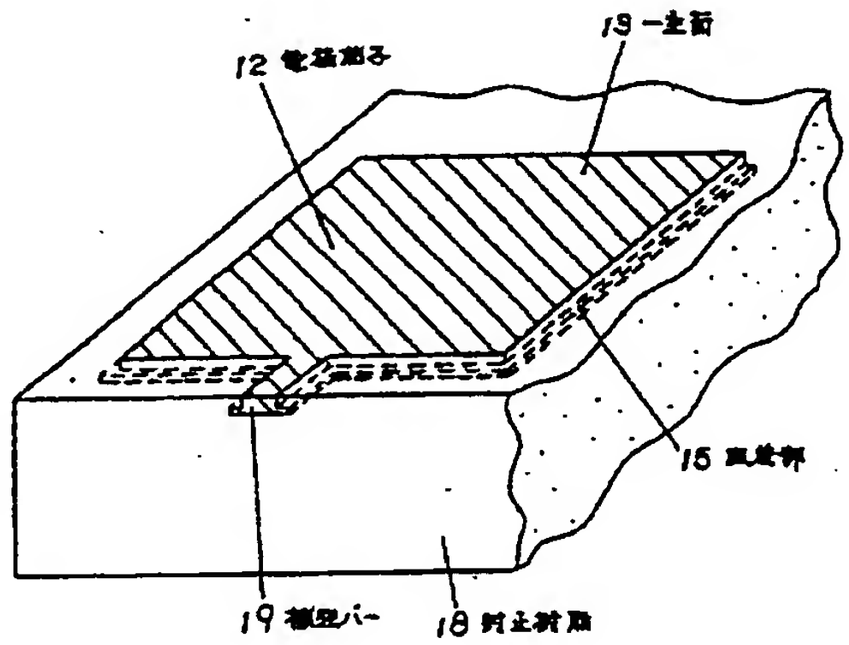
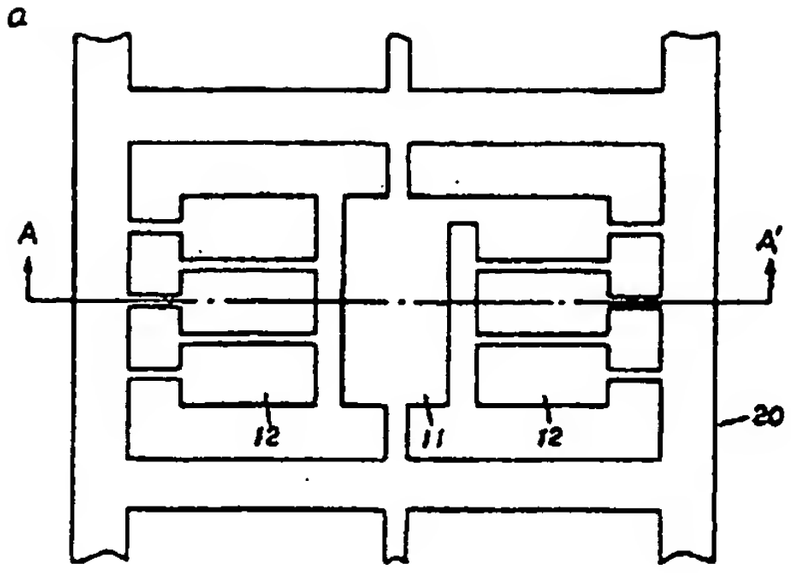


Figure 1

Key: 12 Electrode terminal
13 One principal surface
15 Step
18 Sealing resin
19 Reinforcing bar



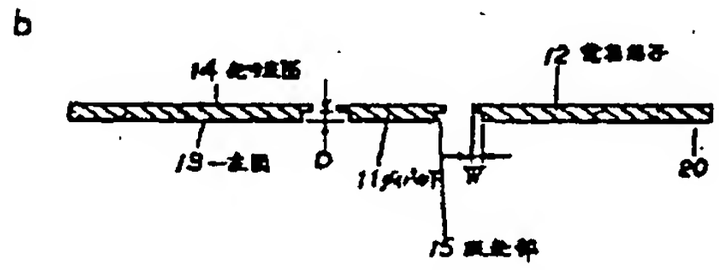


Figure 2

Key: 11 Die pad
12 Electrode terminal
13 One principal surface
14 Other principal surface
15 Step

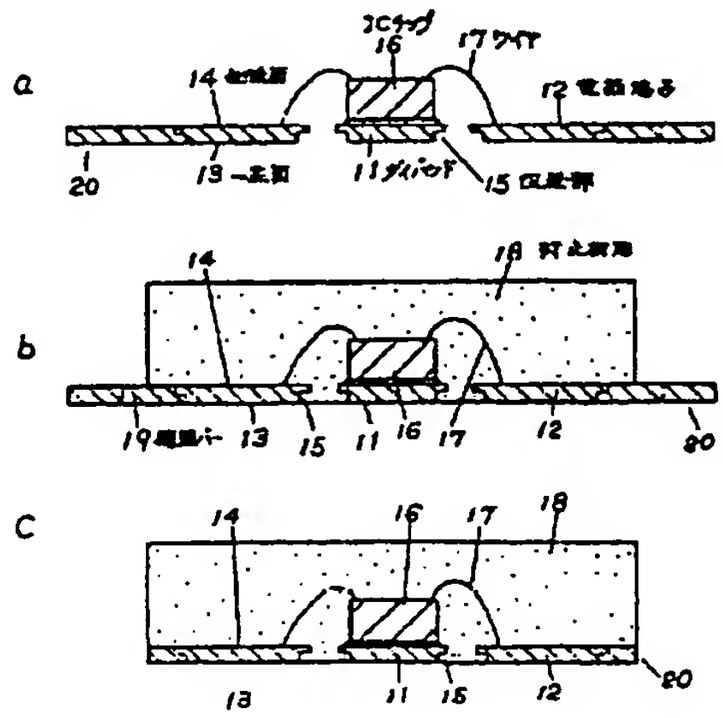


Figure 3

Key: 11 Die pad
12 Electrode terminal

13 One principal surface
14 Other principal surface
15 Step
16 IC chip
17 Wire
18 Sealing resin
19 Reinforcing bar

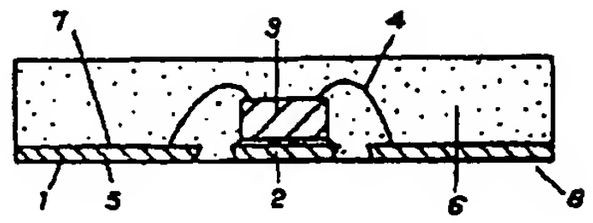


Figure 4

RALPH
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April 5, 2004

Re: RMTC Job No. 2098-96421

To Whom It May Concern:

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- Japanese Patent: JP 1-106456 [JP01106456(A).pdf]

We certify that the attached **English** translation (2098-96421.doc) conforms essentially to the original **Japanese** language.

Kim Vitray
Operations Manager

Subscribed and sworn to before me this 5TH day of APRIL 2004.

TINA WUELFING
Notary Public
State of Texas
My Commission Expires
December 8, 2007

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